

# NVMFS5832NL

## Power MOSFET

40 V, 4.2 mΩ, 120 A, Single N-Channel

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- NVMFS5832NLWF – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	40	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	Steady State	$T_{mb} = 25^\circ\text{C}$	$I_D$ 120	A
		$T_{mb} = 100^\circ\text{C}$	84	
Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)	Steady State	$T_{mb} = 25^\circ\text{C}$	$P_D$ 127	W
		$T_{mb} = 100^\circ\text{C}$	64	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 4)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ 21	A
		$T_A = 100^\circ\text{C}$	15	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 3)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$ 3.7	W
		$T_A = 100^\circ\text{C}$	1.9	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$ 557	A	
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	120	A	
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}, V_{GS} = 10 \text{ V}, I_{L(pk)} = 52 \text{ A}, L = 0.1 \text{ mH}, R_G = 25 \Omega$ )	$E_{AS}$	134	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) – Steady State (Notes 2, 3)	$R_{\Psi J-mb}$	1.2	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	40	

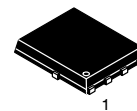
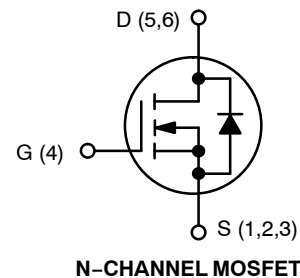
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi ( $\Psi$ ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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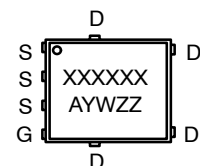
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	4.2 mΩ @ 10 V	120 A
	6.5 mΩ @ 4.5 V	



DFN5  
(SO-8FL)  
CASE 488AA  
STYLE 1

### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVMFS5832NL

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			34.2		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25^\circ\text{C}$		1	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.4		2.4	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			6.4		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		3.1	4.2	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		5.0	6.5	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		21		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$		2700		pF
Output Capacitance	$C_{OSS}$			360		
Reverse Transfer Capacitance	$C_{RSS}$			250		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 20\text{ V}, I_D = 20\text{ A}$		25		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}, I_D = 20\text{ A}$		51		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 20\text{ V}, I_D = 20\text{ A}$		2.0		
Gate-to-Source Charge	$Q_{GS}$			8.0		
Gate-to-Drain Charge	$Q_{GD}$			12.7		
Plateau Voltage	$V_{GP}$			3.2		V

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 20\text{ V}, I_D = 10\text{ A}, R_G = 1.0\ \Omega$		13		ns
Rise Time	$t_r$			24		
Turn-Off Delay Time	$t_{d(OFF)}$			27		
Fall Time	$t_f$			8.0		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 5\text{ A}$	$T_J = 25^\circ\text{C}$		0.73	1.2	V
			$T_J = 125^\circ\text{C}$		0.57		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 10\text{ A}$		28.6		ns	
Charge Time	$t_a$			14			
Discharge Time	$t_b$			14.5			
Reverse Recovery Charge	$Q_{RR}$			23.4			nC

5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

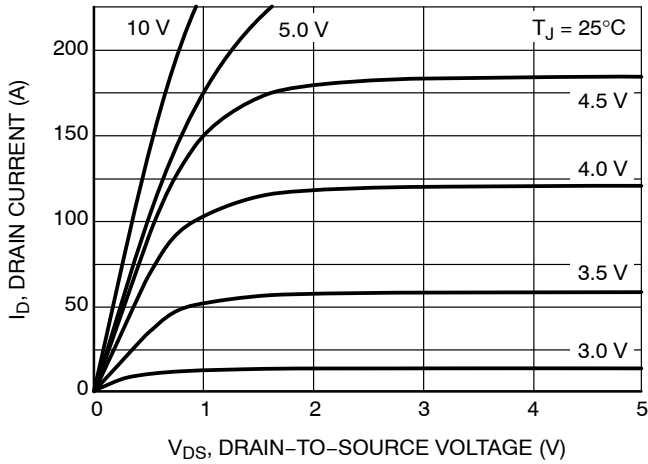


Figure 1. On-Region Characteristics

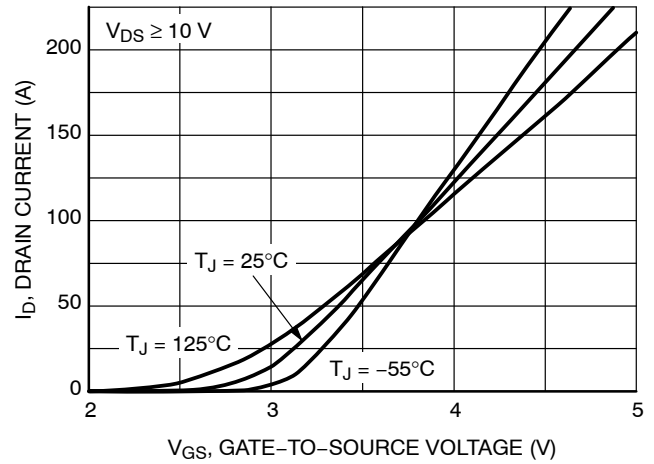


Figure 2. Transfer Characteristics

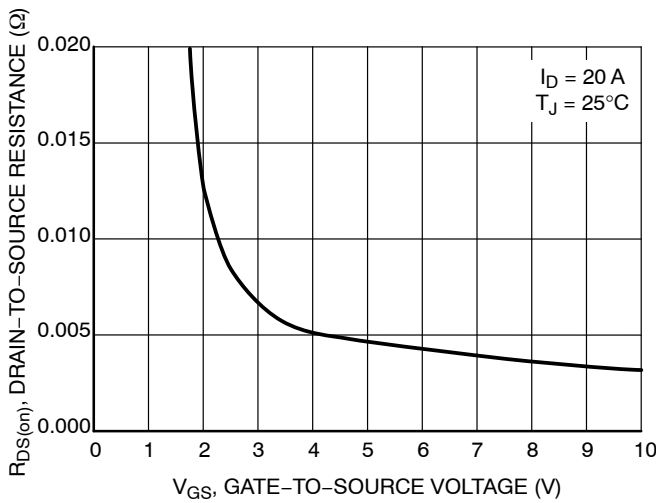


Figure 3. On-Resistance vs. Gate-to-Source Voltage

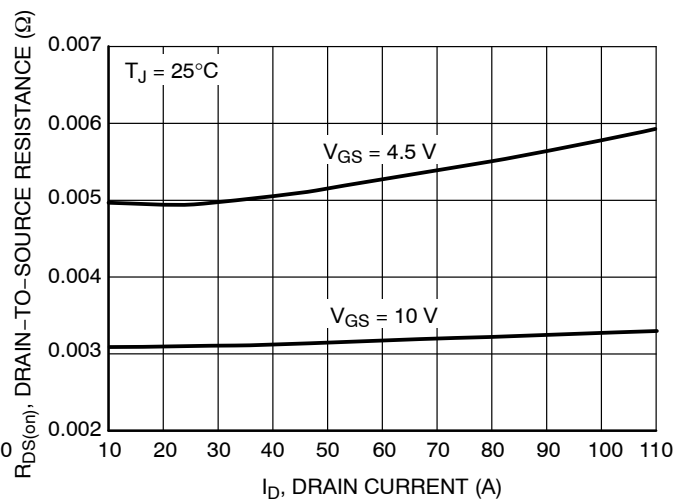


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

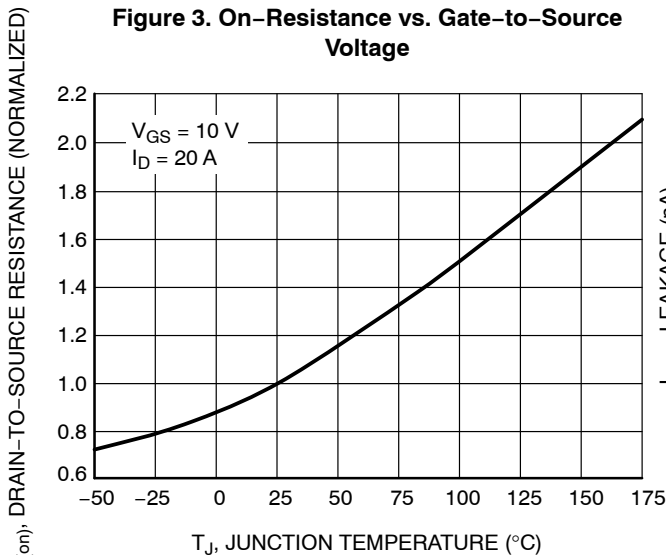


Figure 5. On-Resistance Variation with Temperature

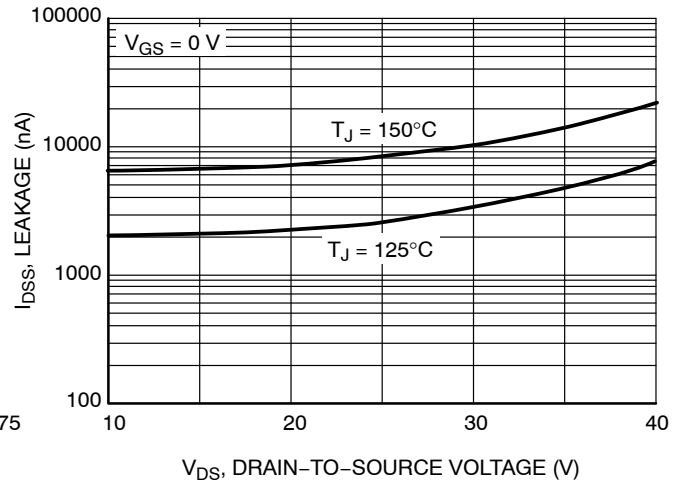


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

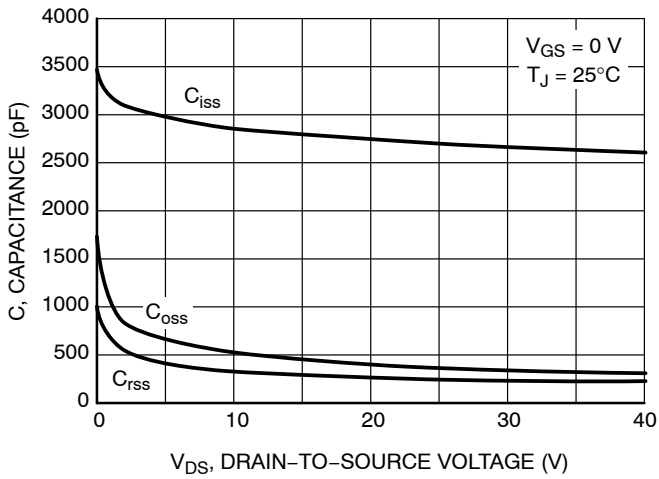


Figure 7. Capacitance Variation

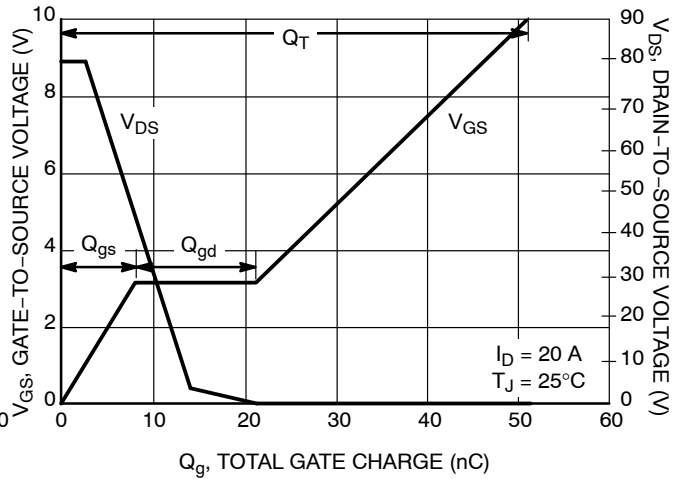


Figure 8. Gate-to-Source Voltage vs. Total Charge

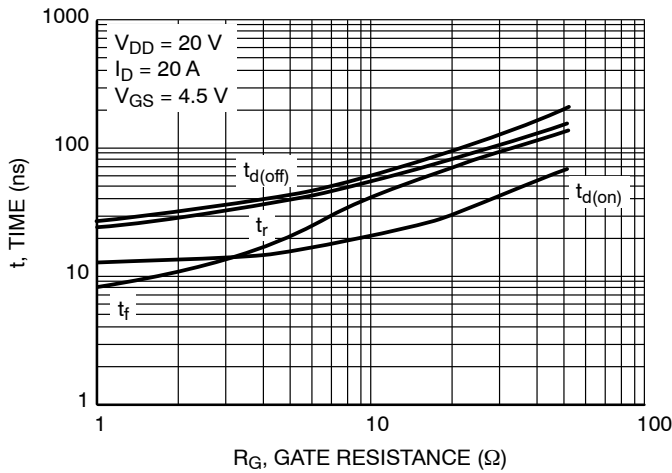


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

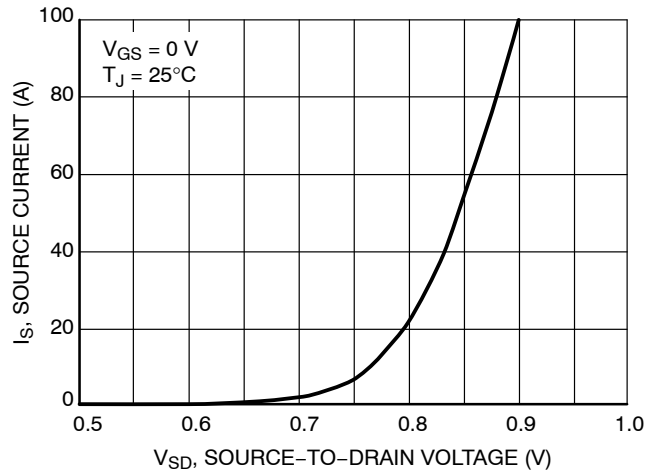


Figure 10. Diode Forward Voltage vs. Current

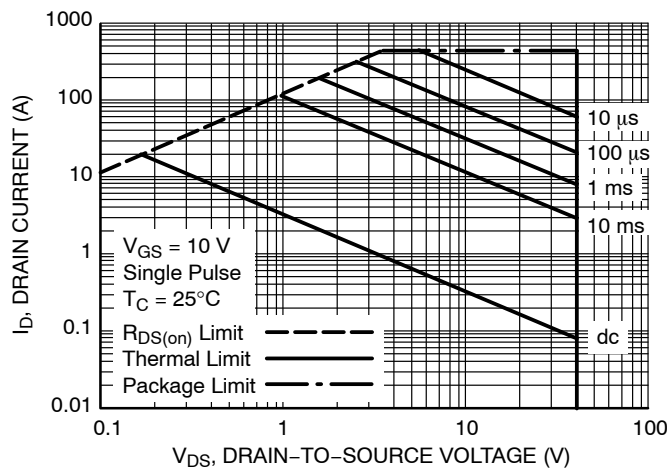


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NVMFS5832NL

## TYPICAL CHARACTERISTICS

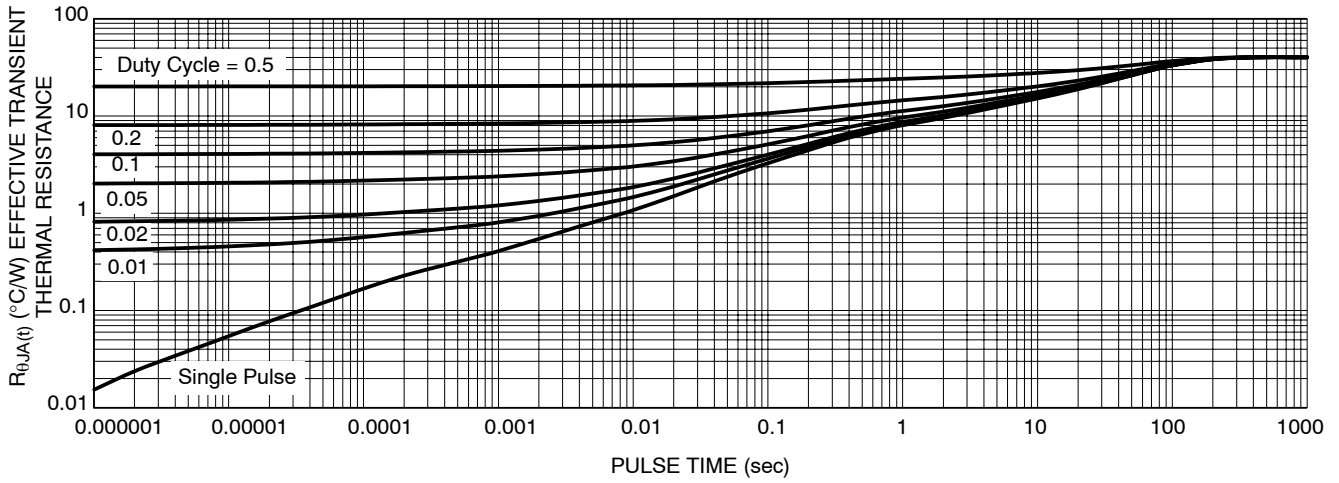


Figure 12. Thermal Response

### DEVICE ORDERING INFORMATION

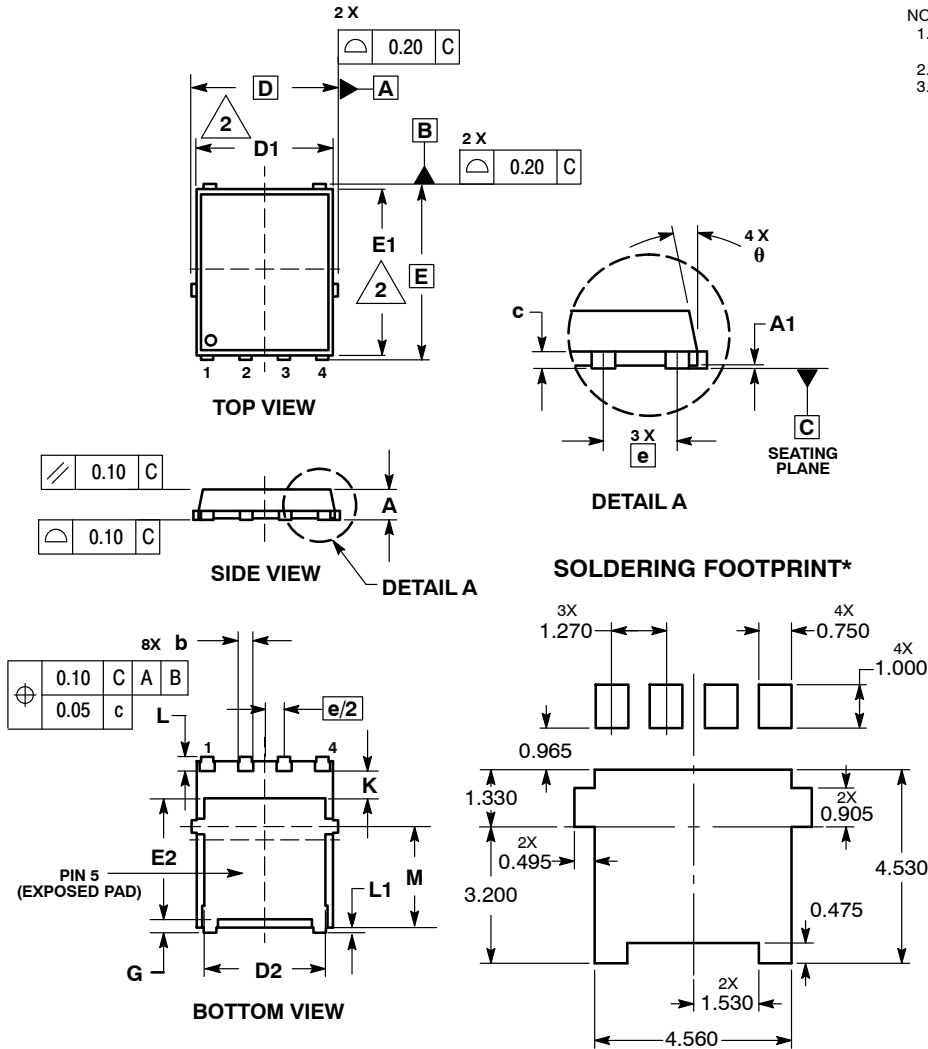
Device	Marking	Package	Shipping <sup>†</sup>
NVMFS5832NLT1G	V5832L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5832NLWFT1G	5832LW	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5832NLT3G	V5832L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5832NLWFT3G	5832LW	DFN5 (Pb-Free)	5000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NVMFS5832NL

## PACKAGE DIMENSIONS

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE H



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0°	---	12°

### STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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